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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/727,102	BARRENSCHEEN ET AL.	
	Examiner	**Art Unit**	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-4,6-20 and 22-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-4,6-20 and 22-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO ARGUMENTS

1. Applicant's arguments filed 04/18/2007 have been fully considered but they are not persuasive. Currently, claims 1, 5 and 21 are canceled and claims 2-4, 6-20 and 22-25 are pending for examination.

2. In response to applicant's argument, on page 9, last paragraph to page 10, 2nd paragraph, regarding the amended claims 23-25 that the combination of references does not teach/suggest every claimed limitations because Balasundram data are encoded utilizing pulse width or pulse amplitude modulation, therefore data are not transmitted in units of frames; and because Balasundram's data are transferred in unit of messages, where each message is intended for a single device, therefore a single message can not be intended for two different devices; applicant's arguments have fully been considered, but are not found to be persuasive.

The encoding of data utilizing pulse width or pulse amplitude modulation is one of the embodiments that Balasundram teaches, the examiner is actually relying specifically on Balasundram's teaching of the embodiments relating to the transferring of data utilizing time division multiplexing (TDM) ([0006] and [0008]-[0009]). The examiner is not relying on Balasundram's teaching of pulse width or pulse amplitude modulation on paragraph [0007], but is relying on paragraph [0007] for the teaching that a single transmitter (e.g. single center transmitter) is transmitting data to multiple receivers.

Additionally, Balasundram teaches the transferring of data between a remote vehicle system controller (e.g. single transmitter) and a plurality of vehicle functions (e.g. plurality of receivers), wherein the transferring of data is utilizing a series of time intervals by utilizing TDM ([0046]).

Please note that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). As in the instant application, the amended claimed limitation " wherein the load control data and the pilot data are transmitted in units of frames, and wherein the load control data frames and the pilot data frames are transmitted using time-division multiplexing; and wherein a first portion of data transmitted in a frame is intended for a first, second semiconductor chip, and a second portion of the data transmitted in this frame is intended for a second, second semiconductor chip" would have been obvious in view of the combined teaching of AAPA and Balasundram, wherein the examiner relied on the references as following for the teaching of the amended claimed limitation:

AAPA teaches an arrangement comprising:

a first semiconductor chip (Drawings, MC of Fig. 1 and Specification, [0002]-[0003]); and

a second semiconductor chip (Drawings, PC of Fig. 1 and Specification, [0002]-[0003]) which is connected to and drives electrical loads based on a timing defined by load control data (Specification, [0002] and [0004]-[0005]);

transferring of a load control data and a pilot control data from the first semiconductor chip to the second semiconductor chip (Specification, [0002] and [0008]-[0009]), where the each data is transferring utilizing a load control data line and a pilot data line respectively.

Balasundram teaches a system and a method comprising

transferring two or more messages (e.g. data) on the same communication line, by utilizing multiplexing technique such as time division multiplexing ([0006] and [0008]-[0009]);

wherein the transferring of data is send from a single central transmitter to the plurality of receivers ([0007] and [0046]), as data is transferred between a remote vehicle system controller (e.g. single transmitter) and a plurality of vehicle functions (e.g. plurality of receivers); and

wherein the plurality of data are transferred via an allotted particular time interval (e.g. units of frames) ([0008] and [0046]), wherein it would have been obvious for the plurality of data to be transferred utilizing a single allotted time interval (e.g. single frame), therefore the single allotted time interval is utilized for transferring the plurality of data (frames).

By combining Balasundram with AAPA, the resulting combination of reference further teaches the arrangement comprising:

transferring two or more data (e.g. load control data and pilot control data) on the same communication line utilizing time division multiplexing in the allotted particular time interval (e.g. units of frames); and

by transferring the plurality of data utilizing the single allotted time interval (e.g. frame), it would have been obvious that in the single allotted time interval, the first portion of the allotted time interval having the first data directed towards a first receiver (e.g. first, second semiconductor chip) and a second portion of the time interval having the second data directed towards a second receiver (e.g. second, second semiconductor chip).

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

3. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

4. The applicant's drawings submitted are acceptable for examination purposes.

III. OBJECTIONS TO THE CLAIMS

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 6-9 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 6 and 22, it appears unclear regarding the dependency for each respective claim, as the claims are dependent on canceled claim 5. The examiner will assume that each respective claim is dependent on claim 23 for the examination.

Claims 7-9 are rejected at least due direct or indirect dependency on the rejected claim 6.

IV. <u>REJECTIONS BASED ON PRIOR ART</u>

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-4, 6-8, 10, 12 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (<u>AAPA</u>) in view of <u>Balasundram et al.</u> (US Pub.: 2003/0103519).

7. As per claims 23-24, <u>AAPA</u> teaches an arrangement comprising:

a first semiconductor chip (Drawings, MC of Fig. 1 and Specification, [0002]-[0003]); and

a second semiconductor chip (Drawings, PC of Fig. 1 and Specification, [0002]-[0003]) which is connected to and drives electrical loads based on a timing defined by load control data (Specification, [0002] and [0004]-[0005]);

a first data communication means for the second semiconductor chip transmitting diagnostic data, which represent at least one of states prevailing in and events occurring in the second semiconductor chip, to the first semiconductor chip (Specification, [0002] and [0011]);

a load control data line (Drawings, DATA2 of Fig. 1) utilized by the first semiconductor chip transmitting the load control data which control the second semiconductor chip (Specification, [0002] and [0008]-[0009]); and

a pilot data line (Drawings, DATA1a of Fig. 1) utilized by the first semiconductor chip transmitting the pilot data which control the second semiconductor chip (Specification, [0002] and [0008]-[0009]).

<u>AAPA</u> does not teach the arrangement comprising:

the plurality of second semiconductor chips;

a single, second data communication means for the first semiconductor chip transmitting the load control data and pilot data; and

wherein the load control data and the pilot data are transmitted in units of frames, and wherein the load control data frames and the pilot data frames are transmitted using time-division multiplexing; and

wherein a first portion of data transmitted in a frame is intended for a first, second semiconductor chip, and a second portion of the data transmitted in this frame is intended for a second, second semiconductor chip

Balasundram teaches a system and a method comprising:

transferring two or more messages (e.g. data) on the same communication line, by utilizing multiplexing technique such as time division multiplexing (TDM) ([0006] and [0008]-[0009]);

wherein the transferring of data is sent from a single central transmitter to the plurality of receivers ([0007] and [0046]), as data is transferred between a remote vehicle system controller (e.g. single transmitter) and a plurality of vehicle functions (e.g. plurality of receivers); and

wherein the plurality of data are transferred via an allotted particular time interval (e.g. units of frames) ([0008] and [0046]), wherein it would have been obvious for the plurality of data to be transferred utilizing a single allotted time interval (e.g. single frame), therefore the single allotted time interval is utilized for transferring the plurality of data.

Balasundram is analogous art because Balasundram is reasonably pertinent to the particular problem with which the applicant was concerned, which is transferring data over a single communication line utilizing time division multiplexing, therefore reducing the number of communication lines needed.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Balasundram's transferring of data utilizing TDM into

AAPA's arrangement. The resulting combination of the references further teaches the arrangement comprising

the single transmitter (e.g. first semiconductor chip) is transferring data to the plurality of receivers (e.g. plurality of second semiconductor chips);

transferring two or more data (e.g. load control data and pilot control data) on the same communication line utilizing time division multiplexing in the allotted particular time interval (e.g. units of frames); and

by transferring the plurality of data utilizing the single allotted time interval (e.g. frame), it would have been obvious that in the single allotted time interval, the first portion of the allotted time interval have the first data directed towards a first receiver (e.g. first, second semiconductor chip) and the second portion of the time interval have the second data directed towards a second receiver (e.g. second, second semiconductor chip).

The suggestion/motivation for doing so would have been for the benefit of reducing the overall number of wires utilized (Balasundram, [0006]).

Therefore, it would have been obvious to combine Balasundram with AAPA for the benefit of reducing the overall number of wires utilized to obtain the invention as specified in claims 23-24.

8. As per claim 25, AAPA teaches a method for communicating in an arrangement having a first semiconductor chip (Drawings, MC of Fig. 1) and a second semiconductor

chip (Drawings, PC of Fig. 1) which is connected to and drives electrical loads based on a timing defined by load control data (Specification, [0002]-[0003]), comprising:

the second semiconductor chip transmitting diagnostic data, which represent at least one of states prevailing in and events occurring in the second semiconductor chip, via a first data line (Drawings, DATA1b of Fig. 1) to the first semiconductor chip (Specification, [0002] and [0011]);

the first semiconductor chip transmitting the load control data, which control the second semiconductor chip, via a load control data line (Drawings, DATA2 of Fig. 1) (Specification, [0002] and [0008]-[0009]); and

the first semiconductor chip transmitting the pilot data, which control the second semiconductor chip, via a pilot data line (Drawings, DATA1a of Fig. 1) (Specification, [0002] and [0008]-[0009])

AAPA teaches the method comprising

the plurality of second semiconductor chips;

the transmission of the load control data and pilot data is implemented via a single, second data line;

wherein the load control data and the pilot data are transmitted in units of frames, and wherein the load control data frames and the pilot data frames are transmitted using time-division multiplexing; and

wherein a first portion of data transmitted in a frame is intended for a first, second semiconductor chip, and a second portion of the data transmitted in this frame is intended for a second, second semiconductor chip

Balasundram teaches a system and a method comprising:

transferring two or more messages (e.g. data) on the same communication line, by utilizing multiplexing technique such as time division multiplexing (TDM) ([0006] and [0008]-[0009]);

wherein the transferring of data is send from a single central transmitter to the plurality of receivers ([0007] and [0046]), as data is transferred between a remote vehicle system controller (e.g. single transmitter) and a plurality of vehicle functions (e.g. plurality of receivers); and

wherein the plurality of data are transferred via an allotted particular time interval (e.g. units of frames) ([0008] and [0046]), wherein it would have been obvious for the plurality of data to be transferred utilizing a single allotted time interval (e.g. single frame), therefore the single allotted time interval is utilized for transferring the plurality of data.

Balasundram is analogous art because Balasundram is reasonably pertinent to the particular problem with which the applicant was concerned, which is transferring data over a single communication line utilizing time division multiplexing, therefore reducing the number of communication lines needed.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Balasundram's transferring of data utilizing TDM into AAPA's arrangement. The resulting combination of the references further teaches the arrangement comprising

the single transmitter (e.g. first semiconductor chip) is transferring data to the plurality of receivers (e.g. plurality of second semiconductor chips);

transferring two or more data (e.g. load control data and pilot control data) on the same communication line utilizing time division multiplexing in the allotted particular time interval (e.g. units of frames); and

by transferring the plurality of data utilizing the single allotted time interval (e.g. frame), it would have been obvious that in the single allotted time interval, the first portion of the allotted time interval have the first data directed towards a first receiver (e.g. first, second semiconductor chip) and the second portion of the time interval have the second data directed towards a second receiver (e.g. second, second semiconductor chip).

The suggestion/motivation for doing so would have been for the benefit of reducing the overall number of wires utilized (Balasundram, [0006]).

Therefore, it would have been obvious to combine Balasundram with AAPA for the benefit of reducing the overall number of wires utilized to obtain the invention as specified in claim 25.

9. As per claim 2, AAPA and Balasundram teach all the limitations of claim 23 as discussed above, where AAPA further teaches the arrangement comprising wherein the first semiconductor chip is a program-controlled unit (AAPA, Drawings, MC of Fig. 1).

10. As per claim 3, AAPA and Balasundram teach all the limitations of claim 23 as discussed above, where AAPA further teaches the arrangement comprising wherein the second semiconductor chip is a power chip (AAPA, Drawings, PC of Fig. 1).

11. As per claim 4, AAPA and Balasundram teach all the limitations of claim 23 as discussed above, where AAPA further teaches the arrangement comprising wherein the second data line is part of a second transmission channel which comprises:

a transmission clock line (AAPA, Drawings, CLK1, CLK2 of Fig. 1) via which the first semiconductor chip transmits a transmission clock signal to the second semiconductor chip (AAPA, Specification, [0021]-[0022] and [0024]-[0025]);

the second data line via which the first semiconductor chip transmits the load control data and the pilot data to the second semiconductor chip in time with the transmission clock signal (AAPA, Specification, [0021]-[0022] and [0024]-[0025]); and

a chip select line (AAPA, Drawings, CS1, CS2 of Fig. 1) via which the first semiconductor chip transmits the chip select signal to the second semiconductor chip, the chip select signal signaling to the second semiconductor chip the start and end of the transmission of data intended for the second semiconductor chip via the second data line (AAPA, Specification, [0021]-[0022] and [0024]-[0025]).

12. As per claim 6, AAPA and Balasundram teach all the limitations of claim 23 as discussed above, where AAPA further teaches the arrangement comprising wherein the first semiconductor chip defines time windows (e.g. a particular time interval) of constant

length and transmits in each time window either the load control data frame or the pilot data frame or no data (AAPA, Specification, [0002]-[0005] and [0008]-[0009]), as the microcontroller (i.e. first semiconductor chip) controls and configures the power chip (i.e. second semiconductor chip) and that the power chip does nothing other than drive the electrical loads base on the stipulation received from the microcontroller, it would then be obvious for the microcontroller to define the time windows for transferring the corresponding data.

13. As per claim 7, AAPA and Balasundram teach all the limitations of claim 6 as discussed above, where both further teaches the arrangement comprising wherein the first semiconductor chip transmits no further load control data frame for a respective length of n time windows after transmission of a load control data frame, where $n \geq 0$ and where n can be set by the user of the arrangement (AAPA , Specification, [0008]-[0009] and Balasundram, [0014], [0039]), as the multiplexing operates in a cyclical manner and the transferred message may have up to six instructive frames (Balasundram, Fig. 1, ref. 24-34), wherein the message is operate repetitively; therefore, the transferring of data may comprise the load control data frame following by the pilot data frame for configuring the second semiconductor into the sleep mode, thus the transferring of the load control data frame may have been stopped for the period of $n \geq 0$ frame, as the second semiconductor is in the sleep mode.

14. As per claim 8, AAPA and Balasundram teach all the limitations of claim 7 as discussed above, where Balasundram further teaches the arrangement comprising wherein a pilot data frame can be transmitted only in a time window in which no load control data frame is to be transmitted (Balasundram, Fig. 1 and [0008]), as each frame is allocated for a particular time interval, wherein each interval is for transferring a single message; therefore while the load control data frame is being transferred, the pilot data frame can not be transferred and vice versa.

15. As per claim 10, AAPA and Balasundram teach all the limitations of claim 23 as discussed above, where Balasundram further teaches the arrangement comprising wherein the first data line is part of a first transmission channel, and the first data line is used to transmit neither load control data nor pilot data (Balasundram, [0006]-[0009]), as the load control data and the pilot data are to be multiplexed over the single second communication line, therefore the transferring of these data would not utilize the first data line.

16. As per claim 12, AAPA and Balasundram teach all the limitations of claim 23 as discussed above, where AAPA further teaches the arrangement comprising wherein the first semiconductor chip transmits appropriate pilot data in order to prescribe to the second semiconductor chip what transmission rate is to be used by the second semiconductor chip to transmit the diagnostic data to the first semiconductor chip (AAPA, Specification, [0009]), as the pilot data is utilized for setting the second

semiconductor chip in modes including normal mode and sleep mode, therefore the corresponding mode, set by the pilot data would prescribe the transmission rate of the diagnostic data, such as having the normal rate during the normal mode or having the lower rate during the sleep mode.

17. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Balasundram et al. (US Pub.: 2003/0103519) as applied to claim 6 above, and further in view of Jones et al. (US Patent 3,985,962).

AAPA and Balasundram teach all the limitations of claim 6 as discussed above, but AAPA and Balasundram does not expressly teaches the arrangement comprising wherein transmission of the pilot data has priority when load control data and pilot data are awaiting transmission simultaneously.

Jones teaches a system and a method comprising a priority scheme such that when service request occurs simultaneous, the one with the higher priority is serviced prior to the others having lower priority (col. 1, ll. 15-37).

Jones is analogous art because Jones is reasonably pertinent to the particular problem with which the applicant was concerned, which is related to the transferring of data utilizing TDM.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Jones's priority scheduling into AAPA and Balasundram's apparatus. The resulting combination of the references further teaches the apparatus comprising when transferring of load control data and pilot data occurs

simultaneous, pilot data would have higher priority to be transferred before transferring the load control data, because the pilot data is utilized for configuring the operation of the second semiconductor chip; such that, when the second semiconductor chip is in sleep mode and the attempt to transfer load control data and pilot data occurs simultaneous, the pilot data would need to be transferred first to configure the second semiconductor to normal mode (e.g. awake mode) before sending the load control data for processing and execution.

The suggestion/motivation for doing so would have been for the benefit of enabling the proper processing of simultaneous request in the system utilizing time-division multiplexing communication (Jones, col. 1, ll. 15-37).

Therefore, it would have been obvious to combine Jones with AAPA and Balasundram for the benefit of enabling the proper processing of simultaneous request in the system utilizing time-division multiplexing communication to obtain the invention as specified in claim 9.

18. Claims 11, 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Balasundram et al. (US Pub.: 2003/0103519) as applied to claim 23 above, and further in view of "Data Communications Basics".

19. As per claims 11 and 17, AAPA and Balasundram teach all the limitations of claim 23 as discussed above, where AAPA further teaches the arrangement comprising wherein the transmission of data (AAPA, Drawings, DATA1a, DATA2 of Fig. 1) is

accompany by the corresponding clock signal (AAPA, Drawings, CLK1, CLK2 of Fig. 1), as the first semiconductor chip (e.g. master) transmits the transmission clock signal to the second semiconductor chip (e.g. slave) (AAPA, Specification, [0021]-[0022] and [0024]-[0025]).

AAPA and Balasundram does not expressly teach the arrangement wherein the diagnostic data are transmitted in synch with a transmission clock signal generated in the second semiconductor chip and wherein this transmission clock signal is not transmitted to the first semiconductor chip; and wherein the second semiconductor chip transmits the diagnostic data in synch with the transmission clock signal received from the first semiconductor chip

"Data Communications Basics" teaches a communication system and method comprising the receiver (i.e. second semiconductor chip) receiving the transmitter's internal clock (i.e. first semiconductor chip's transmission clock signal) and the transmitter's data, the receiver then synchronizes the receiver's local oscillator to the transmitter's local oscillator, wherein said receiver's local oscillator generates the respective receiver's internal clock (i.e. second semiconductor chip's transmission clock) and the data generated by the receiver to be transmitted to the transmitter utilizes the receiver's internal clock, therefore said data generated by the receiver would be in synch with the transmitter's internal clock, wherein the receiver does not transmit the receiver's internal clock to the transmitter (i.e. first semiconductor chip) (Asynchronous vs. Synchronous Transmission Section on page 4).

Data Communications Basics are analogous art because Data Communications Basics is reasonably pertinent to the particular problem with which the applicant was concerned, which is to transferring the plurality of data serially via time frames.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Data Communications Basics' communication system and method into AAPA and Balasundram's arrangement.

The suggestion/motivation for doing so would have been for the benefit of providing a more robust asynchronous data transferring and receiving system and method.

Therefore, it would have been obvious to combine "Data Communications Basics" with AAPA and Balasundram for the benefit of providing a more robust asynchronous data transferring and receiving system and method to obtain the invention as specified in claims 11 and 17.

20. As per claim 15, AAPA, Balasundram and "Data Communications Basics" teach all the limitations of claim 11 as discussed above, where Balasundram further teaches the arrangement comprising wherein the diagnostic data are transmitted in units of frames (e.g. particular time interval) (Balasundram, [0008]), where a frame starts with a start bit (e.g. leading component of "1") (Balasundram, Fig. 3, ref. 52) having a prescribed value and ends with one or two stop bits (Balasundram, Fig. 3, ref. 58) having prescribed values (e.g. having value of "0") (Balasundram, [0039] and [0042]-[0043]).

21. Claims 13-14 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Balasundram et al. (US Pub.: 2003/0103519) as applied to claims 12 and 23 above, and further in view of Hastings et al. (US Patent 6,772,251).

22. As per claim 13, AAPA and Balasundram teach all the limitations of claim 12 as discussed above.

AAPA and Balasundram does not expressly teach the arrangement comprising wherein the transmission rate is prescribed by transmitting a division factor, and wherein the second semiconductor chip (e.g. slave) divides the frequency of a transmission clock signal transmitted to it by the first semiconductor chip (e.g. master) by the division factor and transmits the diagnostic data to the first semiconductor chip in time with the resultant signal.

Hastings teaches a system and a method for transferring serial data between a master (Fig. 1, ref. 110) and a slave (Fig. 1, ref. 120), comprising of a clock divider (Fig. 1, ref. 122) at the slave for dividing down the clock frequency from the master, and transfer data from the slave to the master using this resulting clock frequency (Fig. 1, col. 1, ll. 29-36; col. 2, ll. 60-67 and col. 3,ll. 1-21).

Hastings is analogous art because Hastings is reasonably pertinent to the particular problem with which the applicant was concerned, which is to transferring the plurality of data serially over a single communication line via time frames

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Hastings's division of the clock into AAPA and Balasundram's arrangement.

The suggestion/motivation for doing so would have been for the benefit of reducing the number of wires needed and increase data flow by reducing the flow of start and stop bits (Hastings, col. 1, ll. 29-55).

Therefore, it would have been obvious to combine Hastings with AAPA and Balasundram for the benefit of reducing the number of wires needed and increase data flow by reducing the flow of start and stop bits to obtain the invention as specified in claim 13.

23. As per claim 14, AAPA, Balasundram and Hastings teach all the limitations of claim 13 as discussed above, where AAPA further teaches teach the arrangement comprising the transmission clock signal supplied to the second semiconductor chip (e.g. slave) represent the transmission clock, which is used by the first semiconductor chip (e.g. master) to transmit the load control data or pilot data signal to the second semiconductor chip (e.g. slave) (AAPA, Drawings, CLK1, CLK2, Data1a, Data2 of Fig. 1 and Specification, [0021]-[0025]).

24. As per claim 22, AAPA and Balasundram teach all the limitations of claim 23 as discussed above, where both further teach the arrangement comprising wherein the first semiconductor chip (e.g. single center transmitter) is connected to a plurality of second

semiconductor chips (e.g. receivers) (Balasundram, [0007]), every second semiconductor chip is connected to the first semiconductor chip via a dedicated chip select line (AAPA, Drawings, CS1, CS2 of Fig. 1), and chip select signals transmitted via the chip select lines (AAPA, Specification, [0023] and [0026]).

AAPA and Balasundram does not expressly teach the arrangement comprising wherein the arrangement comprising wherein the chip select signals transmitted via the chip select lines can be altered during the transmission of a frame.

Hastings further teaches an enabling signal (e.g. chip select signal) used by the slave (Fig. 3, ref. 304), wherein the enabling signal initiates the slave for transmission of data to the master and the enabling signal can be transmitted during the transmission of a frame, therefore can be altered from high to low or low to high during the transmission of the frame (Fig. 3, ref. 304).

Hastings is analogous art because Hastings is reasonably pertinent to the particular problem with which the applicant was concerned, which is to transferring the plurality of data serially over a single communication line via time frames

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Hastings's altering of the enable signal into AAPA and Balasundram's arrangement.

The suggestion/motivation for doing so would have been for the benefit of reducing the number of wires needed and increase data flow by reducing the flow of start and stop bits (Hastings, col. 1, ll. 29-55).

Therefore, it would have been obvious to combine Hastings with AAPA and Balasundram for the benefit of reducing the number of wires needed and increase data flow by reducing the flow of start and stop bits to obtain the invention as specified in claim 22.

25. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Balasundram et al. (US Pub.: 2003/0103519) and further in view of and "Data Communications Basics" as applied to claim 11 above, and further in view of Bishop (US Patent 6,154,509).

AAPA, Balasundram and "Data Communications Basics" teach all the limitations of claim 11 as discussed above, but AAPA, Balasundram and "Data Communications Basics" do not expressly teach the arrangement comprising wherein the first semiconductor chip ascertains the phase of the diagnostic data by oversampling the diagnostic data.

Bishop teaches a system and a method comprising a receiver oversampling an inputting signal, therefore able to proper determine the phase of the inputting signal (col. 1, ll. 36-40 and col. 1, ll. 50-55).

Bishop is analogous art because Bishop is reasonably pertinent to the particular problem with which the applicant was concerned, which transferring of data via time-multiplexing.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Bishop's oversampling of the inputting signal into AAPA,

Balasundram and "Data Communications Basics"'s apparatus. The resulting combination of the references further teaches the apparatus comprising wherein the the first semiconductor chip oversampling the received diagnostic data in order to properly determine the correct phase of the received signal.

The suggestion/motivation for doing so would have been for the benefit of providing noise immunity (Bishop, col. 1, l. 57) and reducing cost of the design (Bishop, col. 3, ll. 13-25).

Therefore, it would have been obvious to combine AAA with BBB for the benefit of providing noise immunity and reducing cost of the design to obtain the invention as specified in claim 16.

26. Claims 18-19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Balasundram et al. (US Pub.: 2003/0103519) as applied to claim 23 above, and further in view of Rehmann et al. (US Patent 6,578,940).

27. As per claims 18-19, AAPA and Balasundram teach all the limitations of claim 23 as discussed above, where AAPA further teaches the arrangement comprising wherein the second line is part of a second transmission channel which further comprises:

a transmission clock line (AAPA, Drawings, CLK1, CLK2 of Fig. 1) via which the first semiconductor chip transmits a transmission clock signal to the second semiconductor chip (AAPA, Specification, [0021]-[0022] and [0024]-[0025]);

a chip select line (AAPA, Drawings, CS1, CS2 of Fig. 1) via which the first semiconductor chip transmits a chip select signal to the second semiconductor chip, the chip select signal signaling to the second semiconductor chip the start and end of the transmission of data intended for the second semiconductor chip via the second data line (AAPA, Specification, [0023] and [0026]); and

the first semiconductor chip outputting output the load control data (i.e. DATA2), the pilot data (i.e. DATA1a) and the transmission clock signal (i.e. CLK1, CLK2) (AAPA, Specification, [0020]-[0026]).

AAPA and Balasundram does not teach the arrangement comprising:

a second transmission clock line via which the first semiconductor chip transmits a complementary transmission clock signal to the second semiconductor chip;

a third data line via which the first semiconductor chip transmits a complementary load control data and complementary pilot data to the second semiconductor chip; and

wherein output drivers on the first semiconductor chip are LVDS drivers whose use limits electromagnetic interference.

Rehmann teaches a system and a method comprising:

an electronic controller (Fig. 3, ref. 26) including a low-voltage differential signaling (LVDS) driver (Fig. 3, ref. 56), wherein the LVDS driver produces no spike currents (col. 2, ll. 7-8); and

transferring of data from the electronic controller's LVDS driver (Fig. 3, ref. 52) to a receiver (Fig. 3, ref. 56), wherein the LVDS driver has a non-inverted terminal (Fig. 4, ref. 78) and an inverted terminal (Fig. 4, ref. 80) (Fig. 3 and col. 5, ll. 25-28).

Rehmann is analogous art because Rehmann is in the field of applicant's endeavor, which is the controlling and communication associated with the driver component.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Rehmann's LVDS driver into AAPA and Balasundram's arrangement. The resulting combination of the references further teaches arrangement comprising:

the first semiconductor including the LVDS driver, wherein the LVDS would limits electromagnetic interference as the LVDS driver produces no spike current; and

the LVDS' inverted terminal including the second transmission clock line for transferring the complementary transmission clock signal and the third data line for transmits the complementary load control data and complementary pilot data.

The suggestion/motivation for doing so would have been for the benefit of transferring data at very high rate, up to 1.5 gigabits per seconds and not producing any spike currents (Rehmann, col. 2, ll. 7-9).

Therefore, it would have been obvious to combine Rehmann with AAPA and Balasundram for the benefit of transferring data at very high rate, up to 1.5 gigabits per seconds and not producing any spike currents to obtain the invention as specified in claims 18-19.

28. As per claim 20, AAPA and Balasundram teach all the limitations of claim 23 as discussed above, where both further teach the arrangement comprising wherein the second line is part of a second transmission channel which further comprises:

wherein the first semiconductor chip (e.g. single center transmitter) is coupled to a plurality of receivers for outputting the load control data, the pilot data and a transmission clock signal (AAPA , Specification, [0020]-[0025] and Balasundram, [0007]), and wherein a user of the arrangement is able to set which of the plurality of receivers needs to be used in each case (Balasundram, [0007]), wherein the single center transmitter (i.e. first semiconductor chip) generates the encoded data specifying which of the receiver would receives the data.

AAPA and Balasundram does not expressly reaches the arrangement comprising the first semiconductor chip has a plurality of respective different output drivers for outputting data.

Rehmann teaches a system and a method comprising:

an electronic controller (Fig. 3, ref. 26) including a low-voltage differential signaling (LVDS) driver (Fig. 3, ref. 56), wherein the LVDS driver produces no spike currents (col. 2, ll. 7-8); and

transferring of data from the electronic controller's LVDS driver (Fig. 3, ref. 52) to a receiver (Fig. 3, ref. 56), wherein the LVDS driver has a non-inverted terminal (Fig. 4, ref. 78) and an inverted terminal (Fig. 4, ref. 80) (Fig. 3 and col. 5, ll. 25-28).

Rehmann is analogous art because Rehmann is in the field of applicant's endeavor, which is the controlling and communication associated with the driver component.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Rehmann's LVDS driver into AAPA and Balasundram's arrangement. The resulting combination of the references further teaches arrangement comprising wherein the first semiconductor includes the LVDS driver for outputting the data to the respective second semiconductors.

The suggestion/motivation for doing so would have been for the benefit of transferring data at very high rate, up to 1.5 gigabits per seconds and not producing any spike currents (Rehmann, col. 2, ll. 7-9).

Therefore, it would have been obvious to combine Rehmann with AAPA and Balasundram for the benefit of transferring data at very high rate, up to 1.5 gigabits per seconds and not producing any spike currents to obtain the invention as specified in claim 20.

V. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 2-4, 6-20 and 22-25 have received a final action on the merits. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

June 19, 2007

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

Donald Sparks

DONALD SPARKS
SUPERVISORY PATENT EXAMINER